

Implementation Experience of URTDSM Project in Indian Power System

P.K. Agarwal, Rajkumar Anumasula, Chandan Kumar
Power System Operation Corporation Limited
India

SUMMARY

With the evolution of Grid and addition of new power system elements like distributed generation, Grid Scale renewable, energy storage etc., the Indian Power System network has become meshed and complex. The huge demand variation over the day and bidirectional power flow have resulted in introducing new challenges in the form of optimal utilization of the asset and resources. In these dynamic scenarios, it is essential to introduce better monitoring of the power system for the system operator situational awareness. Since last one decade, Synchro phasors has become an effective tool for dynamic monitoring of the power system. Indian Power system has adopted this technology in the year 2010 in the form of pilot projects. After gaining a lot of experience in the utilization of the various pilot projects and associated Synchro phasors data, a full-fledged Synchro phasors Project was designed for Indian Power system which is known as Unified Real Time Dynamic State Measurement System (URTDSM). The URTDSM project includes more than 1400 PMUs in the field and PDCs at 32 State Load Despatch Centre (SLDCs), 5 Regional Load Despatch Centre (RLDCs) and National Load Despatch Centre (NLDC). This paper describes the design and implementation challenges faced during the URTDSM project followed by challenges during its configuration by the system operator. In addition, it described how these issues were resolved in an amicable manner for effective utilization.

KEYWORDS

Synchrophasor, Indian Grid, Wide Area Measurement System,

Introduction

Wide Area Situational Awareness of the power system at sub-second resolution has been introduced in the Indian power system through implementation of regional and national Wide Area Monitoring System (WAMS) pilot projects since 2010 [1-4]. Under these pilot projects, around 64 nos. of PMUs were integrated with National Phasor Data Concentrator (PDC) at NLDC and has been used for Real-time decision making and event analysis. These Pilot projects have been used for fault detection, classification and its analysis, Low frequency oscillations and its mitigation, Coherence group detection, Synchronization and islanding monitoring in the grid, validating the dynamic models, PSS tuning, and Monitoring system during natural disasters etc [1-2]. Based on these WAMS pilot projects experience, a full-fledged Synchrophasor Project was envisaged and implemented in Indian Power System known as Unified Real Time Dynamic State Measurement System (URTDMS) [5]. Presently, under the URTDSM project, about 1444 PMUs are planned and expected to hierarchically report to the thirist two state, five regional and one national control centre. As of now, 1182 PMUs are reporting at National control centre. Data of these PMUs are also being utilized by power system operators as an analytical tool for better system operation in real time.

URTDMS Infrastructure at Control Centre's consists of computer and data storage equipment running a family of tightly coupled software systems supporting central PDC functions, Phasor data management, analysis applications and data historian facilities. In addition, operator workstations running the standalone client visualization software, interface with the central services to provide Phasor data visualization, Wide Area Measurement views and alarm management tools. URTDSM overall architecture in Indian Power System is shown in Figure 1. Typical URTDSM WAMS Control Centre General Architecture Overview. Figure 2 shows the PMUs implemented under URTDSM Phase I across the Indian Power system.

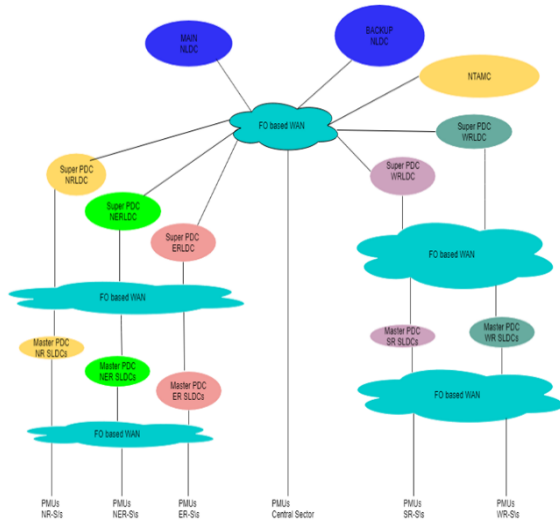


Figure 1: URTDSM architecture in Indian Power System

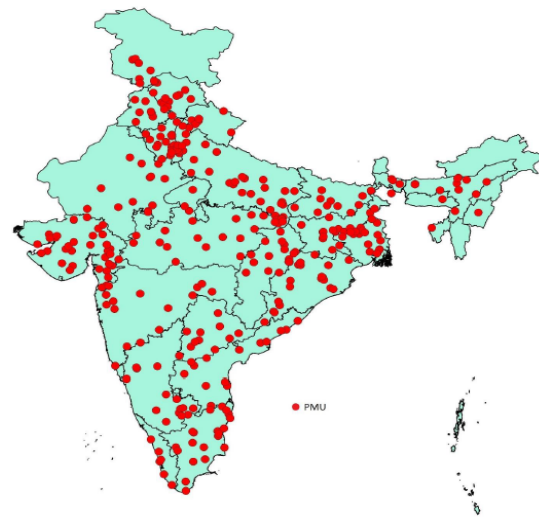


Figure 2: PMU installed under URTDSM Phase I

This paper aims at describing the design and implementation challenges faced during the URTDSM project followed by challenges during its configuration by the system operator. In addition, it describes how these issues were resolved in an amicable manner for effective utilization.

Key Implementation Challenges during URTDSM

With so many PMUs devices installed in the field, the amount of data getting aggregated is huge at control centres. This also provides an opportunity for System operator to observe and address the new challenges faced during the implementation phase of the project for effective utilization of project. Few of the challenges resolved during the implementation of URTDSM project is discussed in this section.

1. Communication Requirement between PDCs at various Control Centre

The Phasor Data Concentrator (PDC) is designed to receive data using the IEEE C37.118 protocol from several numbers of PMUs reporting to State level PDC or Regional Level PDC depending on the jurisdiction [5]. In addition to these, first hierarchical PDCs will be reporting to higher level PDCs at

RLDCs and NLDC. An assessment exercise was done to understand the bandwidth requirements for PMUs and data exchange between PDCs. As per the URTDSM project, each PMU has the capability for 2 Current Transformers (CTs) and 2 Potential Transformers (PTs) configuration, which can be wired for two feeders with one line voltage and one line current per feeder. Accordingly, each feeder data frame as per C37.118.2011 protocol is separately packed with unique ID CODE for the feeder having STAT word (2 Bytes), Phasor (4 Bytes), Frequency (4 Bytes) & ROCOF (4 Bytes), Analog (4 Bytes) and Digital (2 Bytes) which amounts to 52 Bytes [6]. In addition, each PMU stream has SYNC (2 Bytes), ID CODE (2 Bytes), FRACSEC (2 Bytes), SOC (4 Bytes), FRAMESIZE (4 Bytes), CHK (2 Bytes) and TCP Overhead (66 Bytes). A sample bandwidth required for communication links from RLDC PDC to NLDC PDC and NLDC PDC to Backup NLDC PDC envisaged in the URTDSM is shown in Table 1. The sample calculations for single stream between control centres is considered in the shown calculation.

Table 1: Sample Bandwidth Requirement Calculations for Communication System

Sr.No	Region	No.of Substations	No of PMUs	3-Phase Voltage Phasors (Vr, Vy, Vb)	3-Phase Current Phasors (Ir, Iy, Ib)	Positive Sequence Voltage & Current	Digital Inputs (Dis)	Frequency	ROCOF	Analog Values (MW & MVAR)	Inter Control Centre minimum Bandwidth Required in Mbps for each stream @ 25 Frames/sec	Inter Control Centre minimum Bandwidth Required in Mbps for 20% Network load
				6 phasors/ PMU	6 phasors/ PMU	4 phasors /PMU	1 Digital Word /PMU	2 per PMU	2 per PMU	4 per PMU		
1	Northern Region	114	402	2412	2412	1608	402	804	804	1608	14.11	70.56
2	Eastern Region	75	315	1890	1890	1260	315	630	630	1260	11.06	55.29
3	North Eastern Region	14	51	306	306	204	51	102	102	204	1.79	8.95
4	Southern Region	71	270	1620	1620	1080	270	540	540	1080	9.48	47.39
5	Western Region	71	406	2436	2436	1624	406	812	812	1624	14.25	71.26
6	National	345	1444	8664	8664	5776	1444	2888	2888	5776	50.69	253.46

However, for redundant stream configuration, the bandwidth requirement shall be double. If the future network expansion is included then the sample bandwidth will further increase. This exercise has helped in planning of communication system and reducing the data loss in URTDSM.

2. PMU Connection Availability and Data Quality Events & PMU Error statistics

As per the IEEE C37.244 -2013 PDC guide [7], the basic data validation and checking of PMU data correctness including data status flags and time quality, and performing data integrity checks (such as cyclic redundancy check [CRC]) on all received data shall be performed by PDC. Any errors detected and suspected corrupt data should be flagged in the output data stream(s). Similarly, in URTDSM system PDC logs the data quality issues, data errors, validity and Time Quality Issues to Central logging system. PDC Statistics includes PMU Connection Availability, Invalid Data, PMU Time Quality, and PDC Frame through Latency. These statistics provide information on the PMUs Connection availability, GPS synchronization, Communication link bandwidth requirement and data quality issues which helps in troubleshooting.

PMU Connection Availability (in %) is calculated based on the percentage of IEEE C37.118 frames that arrive at an interface for each PMU input stream total number of expected data packets per minute. Once the input stream is started in the PDC and a configuration frame is received, the PDC expects an N number of data packets per second as per 25 Frames/second. If at the network level, one or more packets expected are not received, they will be counted as not available, reducing the percentage of available data in the statistics results. This statistic is important, as it provides details about the communication media level connection and allows network level issues to be diagnosed accurately.

During the Initial phase of commissioning, first level of hierarchical PDCs were only commissioned, and each PMU synchronization statistic was being logged in Central Logging system at respective Control Centre. During the end of commissioning, the next level of hierarchical PDCs (RLDC in case of SLDC PMUs and NLDC in case of RLDC PMUs) have started receiving the PMU data. During this stage, it is observed that PMU Sync Statistics at the second level of PDCs were misleading. For example, even if the PMU was down due to connectivity issue (PMU Availability is 0 %) at first hierarchical level PDC however, PDC statistics at next hierarchical level PDC were showing that GPS is locked to 100 %

which is not correct. To address these kinds of ambiguities in statistics, modified methodologies have been adopted based on different possible permutations and combinations as shown for case 1-3.

Case 1: Individual PMU stream Available at SLDC is 0%, Data Valid is 0%.and GPS Locked is 0%, but SLDC input Stream Available at RLDC is 100%.

In Case 1, PMU's first level reporting is to SLDC PDC and then combined data stream is reporting to RLDC PDC. One such PMU statistics is given in Table 2 where the PMU data is not available at SLDC PDC due to network connectivity issues or due to unplugged PMU network cable. Thus, this PMU data packets will not reach the SLDC PDC and accordingly, SLDC PDC will show 0 % availability. This missing data fails the SLDC PDC wait-time, accordingly, SLDC PDC will send the data packet containing other PMUs reporting at SLDC marking this PMU as absent. So, at the RLDC PDC level, the connection from the SLDC PDC will show 100% available, assuming that there is no data loss between SLDC and RLDC. i.e. the IEEE C37.118 packets were all received for that PDC-PDC connection. However, GPS locked for this PMU was also being reported at RLDC as 100 % which was not true as it is not available. Later with the modified statistics based on PMU non-availability status, it is now being correctly reported as non-available at RLDC PDC level.

Table 2: Hierarchical PDC Data Quality Statistics in Case 1

Typical PMU Data Quality Statistics	Statistics at SLDC PDC	Earlier Statistics at RLDC PDC	Modified Statistics at RLDC PDC
Stream Availability	0%	100%	100%
Data Valid	0%	0%	0%
Data Error	0%	0%	0%
GPS Locked	0%	100%	0%

Case 2: Individual PMU stream Available at SLDC is 100%, Data Valid is 100% & GPS Locked is 100% and SLDC input Stream Data Valid at RLDC is 0% due to delays in the network between RLDC-SLDC.

In this case, PMUs reporting at SLDC PDC is 100 % available and the output stream is provided to RLDC where due to network delays it exceeded RLDC PDC wait time. Due to this the Data Valid and GPS Locked will also be reported as 0 % however stream availability will be marked as 100 %. This helps in identifying the issue is between the communication between two PDCs.

Table 3: Hierarchical PDC Data Quality Statistics in Case 2

Typical PMU Data Quality Statistics	Statistics at SLDC PDC	Statistics at RLDC PDC input
Stream availability	100%	100%
Data Valid	100%	0%
Data Error	0%	0%
GPS Locked	100%	0%

Case 3: Individual PMU stream Available is 90%, Data Valid is 90 % and GPS Locked is 80% at SLDC, but SLDC Stream Data Available is 100%.

In this case 3, stream availability of PMU reporting to SLDC is 90 % due to network delays or any issues however while the same stream if being sent to RLDC will be reported as 100 % available indicating there are no network issues between RLDC and SLDC PDCs. Similarly, the Data validity is marked as 90% at SLDC PDC and 10% data loss at first hierarchical PDC, accordingly next level of PDC also marked the Data Valid as 90%. Same will be the case for the GPS locked quality of PMU being reported at first at SLDC and then to RLDC PDC as shown in table 3.

Table 4: Hierarchical PDC Data Quality Statistics in Case 3

Typical PMU Data Quality Statistics	Statistics at SLDC PDC	Statistics at RLDC PDC input
Stream Availability	90%	100%
Data Valid	90%	90%
Data Error	0%	0%
GPS Locked	80%	80%

The above three cases have illustrated that based on the PDC statistics at several hierarchical levels, it is easy to identify whether the issue is with PMU, Its GPS Locking, Network delays between PMU and PDC or between two hierarchical level PDCs which further helps in troubleshooting.

3. Decoding the PMU Time Synchronization Loss and Data drop from C37.118 flags

As per STAT word of data frame defined in IEEE C37.118.2 -2011 standard, if Bit 13 (PMU Sync Error) is 1 then it indicates that the PMU has detected a loss of external time synchronization such as a loss of satellite tracking or a time input connection failure [6]. It shall be set when the time synchronization input fails and when the source of time synchronization loses lock to UTC traceable time. Further, Bits 6-8 (PMU Time Quality) indicates the maximum uncertainty in the measurement time at the time of measurement which is derived from the time source and needs to be adjusted to include uncertainties in the PMU measuring process [6]. These bits help in finding the issues with time synchronization of PMU and taking corrective action.

PMU Time Synchronization Loss: To illustrate the utilization of STAT word for decoding of the PMU time synchronization loss table 5 and 6 can be referred.

- From Table 5, it can be observed that from 00:00:000 - 00:01:09.120 UTC STAT Bit 13 is set to 1 indicating PMU has lost external time synchronization. During this interval, Bits 6–8 is first set to 111 which indicates that estimated maximum time error > 10 ms or ‘time error unknown’. In addition, Bits 4-5 changes from 00 to 01 at 00:00:09.120 referring that GPS Synchronization unlocking is $10 \text{ sec} \leq \text{unlocked time} < 100 \text{ sec}$, since the loss of synchronization was detected and has elapsed 10 sec.
- At 00:01:09.240 UTC STAT word Bit 13 is set to 0 indicating PMU is synchronized and Bits 6–8 is set to 010 which refers that estimated maximum time error < 1 μs meaning that PMU is synced to its external time synchronization. However, Bits 4–5 remains 01 till 00:01:10.120 UTC i.e. for about one second after clearing Bit 13.
- Same can be verified through latency recorded in PDC log statics shown in below Table 6. It can be found that GPS locked count is 150 out of 1500 frames in a minute considering 25 frames/sec, which constitutes about 10%. Further, PDC is considering “Data valid” for 1500 frames in a minute, although GPS signal is lost for between 00:00:000 - 00:01:09.120 UTC. During this time PMU’s coprocessor internal clock is taking care of the required pulses every second, hence phasor generation and transmission of Synchrophasor streams are continuing to the PDC from PMU.

Table 5: Illustration of Time Sync loss through STAT word of IEEE C37.118 -2011 data frame for a PMU

Time	Status	Frequency in Hz	Bit 15-14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 09	Bit 08 – 06	Bit 05 – 04	Bit 03-00
			[Data Error]	[PMU Sync]	[Data sorting]	[PMU trigger detected]	[Configuration change]	[Data modified]	[PMU Time Quality]	[Unlocked time]	[Trigger reason]
PMU has lost Synchronization as Bit 13 is set to 1 and Estimated maximum time error > 10 ms or time error unknown as Bit 6-8 set as 111											
00:00:00.000	21c0	50.03629	00	1	0	0	0	0	111	00	0000
00:00:09.080	21c0	50.02874	00	1	0	0	0	0	111	00	0000
Estimated maximum time error is >10 s or longer but < 100 s as Bit 5-4 is set as 01											
00:00:09.120	21d0	50.02755	00	1	0	0	0	0	111	01	0000
00:00:54.160	21d0	50.03273	00	1	0	0	0	0	111	01	0000
00:01:09.200	21d8	50.0367	00	1	0	0	0	0	111	01	1000
Bit 13 is set to 010 i.e. GPS is Synchronised, Estimated maximum time error < 1 μs											
00:01:09.240	90	50.0365	00	0	0	0	0	0	010	01	0000
00:01:10.080	90	50.03634	00	0	0	0	0	0	010	01	0000
00:01:10.120	80	50.03611	00	0	0	0	0	0	010	00	0000
00:01:10.200	80	50.03663	00	0	0	0	0	0	010	00	0000
00:01:15.000	8000	NaN	10	0	0	0	0	0	000	00	0000

Table 7: PDC Data Quality Statistics

Time in UTC	% Data Available	% Data Valid	Valid Count	% Error	Error Count	% GPS Locked	GPS Locked Count	Min Ingress latency	Max Ingress Latency	Avg Ingress Latency
00:00:00	100	100	1500	0	0	100	1500	149	155	152
00:01:00	100	100	1500	0	0	10	150	149	180	152
00:02:00	96.8	96.8	1452	0	0	76.133	1142	-851	805	34

PMU Data Dropping: As per Table 6, at 00:01:15:000 UTC Bit 15-14 is set to 10 which indicates that the data from PMU is not valid and PDC has sent to Historian as NaN (not a Number) in line with IEEE C37.118-2011 standard. This is required to be inserted for the absent data in case of the floating format in PDC [6].

4. Negative Latency from PMU:

According to the IEEE PDC Guide C37.244-2013, the most relevant functionalities of a PDC are data aggregation and time alignment which are meant to mitigate the latency variations introduced by the various components of the Synchrophasor network [7-8]. The amount of time the PDC actively waits for data frames with a given time-stamp is called **PDC wait time**, which is crucial to supply dataset to the local applications and the next level of hierarchical PDCs. As per PDC guide, two logics are defined for setting the PDC wait time i.e. **Absolute time logic and Relative time logic**. In Absolute time logic, data pushing is performed once a specific UTC time is reached [7]. While in Relative time logic, the PDC waits for a specified relative time triggered by an event, that could be the arrival of the first data with a specific time-stamp.

URTDMS PDC to Application and Historian server's dataset is supplied through **Relative time logic**. However, this logic fails during the futuristic time stamp measurements arrives at PDC due to some problem with the GPS receiver of the PMU. In one of the cases, few PMUs at one of the Regional Control Centre suddenly stopped reporting as shown in Figure 3. On PMU latency statistics screen of the Regional PDC, three PMUS were showing Negative latency attributed to futuristic PMU time stamp as shown in Figure 4. Due to these three PMUs, Application server driving the operator screens are not receiving all other PMU data due to the fact that maximum wait time has exceeded since the PMU data arrival futuristic time stamp are considered as first data in current time stamp as per the relative time logic. Due to this, it rejects all other PMUs that arrives later than the end of the relative wait time.



Figure 3: Data loss visible from the PMUs in URTDSM Operator screen.

		Ingress Latency			Missing Data Frames	
ID	Status	Min (ms)	Max (ms)	Avg (ms)	Total	Max Consecutive
15007	●	152	166	154	0	0
15010	●	152	166	155	0	0
15013	●	152	166	154	0	0
15016	●	152	166	154	0	0
15202	●	156	211	159	8	3
15205	●	154	203	157	8	3
15208	●	157	216	160	8	3
15211	●	1155	1204	1159	283	25
15214	●	156	208	160	8	3
15217	●	-779	-761	-776	68	25
15220	●	-779	-761	-776	68	25
15223	●	-779	-761	-776	68	25

Figure 4: PDC data Quality Latency Statistics showing negative latency for the last three PMUs

This futuristic time stamp of PMU was also verified with the Wireshark capture as shown in Figure 5 where it can be observed that Arrival Time of Frame is June 07 2019 17:05:30.925083000 India Standard Time (June 07 2019 11:35:30:925 UTC) against PMU SOC Time Stamp of June 07 2019 11:35:31:720 UTC. This means around 795 milliseconds leading timestamp is being sent out by the PMU. Further, there is no time quality errors as shown in Figure 5 and GPS is Locked which also can be viewed from PDC input stream C37.118 Time Quality & PMU Sync Flags from Figure 6.

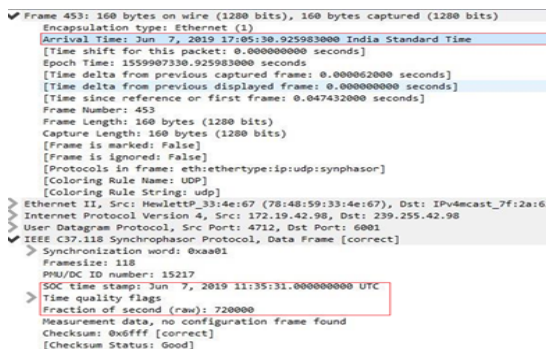


Figure 5: PMU Futuristic Time Stamp verification through Wireshark capture

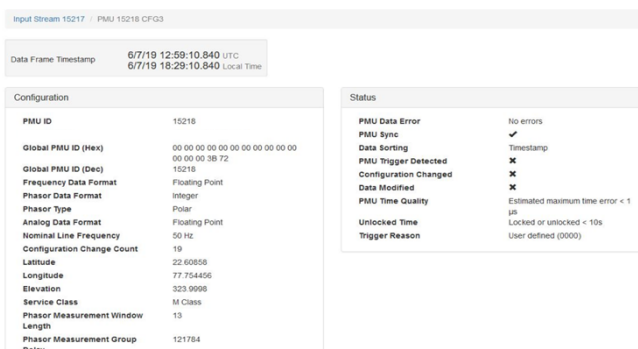


Figure 6: PDC input stream C37.118 STAT flags and time quality view

The above case is a classical case of GPS locked time drifted frame, wherein PMU is time synchronized with GPS and in locked mode, but the locked time is drifted to futuristic timestamps. Typically, PDC is designed to handle Unlocked time drifted frames, where time is drifted due to unlocked GPS. Although PDC has the input side stream rejection for a positive difference of PDC maximum wait time, however

in case of the negative difference, PDC is blind and it will reject the healthy PMUs data considering them as delayed frames. Under such cases, these PMU's streams are blocked till the issues is corrected at PMU level. However, it is always better to handle PDC automatically detect negative latency PMUs in GPS locked drifted frames and reject only these PMU streams.

Challenges in Utilisation of URTDSM

With the implementation of the URTDSM, the next level of challenges was faced during utilization for data for situational awareness of system operator. This has also provided an opportunity to the System operator to address the development of new analytics tool for decision making. Few of the challenges addressed during utilization of URTDSM for Real-time operator are explained in this section.

1. Selection of reference node: Reference node plays a vital role in wide area monitoring as it provides stress monitoring and event detection visualization and alarms to operators. Selection of the reference node is challenging in the large system as requires baselining activities and validation. Prior to the implementation of URTDSM, a baselining activity for reference node on all India basis based on the pilot project was completed and the criteria were defined as given below [9].

Preferred locations for the reference node:

1. Node with strong interconnections and high fault level
2. Nodes with reliable communication
3. Node close to baseload Generation Complex
4. Nodes consistent with offline simulation/EMS studies
5. Node Should be system-wide available and reliable

Nodes to be avoided as Reference node:

1. Nodes with low inertia, weak-tie lines, low fault level
2. Nodes located in oscillation prone area (based on real-time experience)
3. Nodes near to HVDC Bus (varying power order during the day to day operation)
4. Nodes near to varying generation complex

The above criteria have helped operator in the selection of suitable nodes at regional and National control centres. One example of reference node importance is shown in given Figure 7 and Figure 8 wherein if a reference node is selected near to oscillation source and far away from oscillation source are illustrated. It can be observed that if the reference node is node selected appropriately then it directly impact the decision-making process and situational awareness of operator [9].

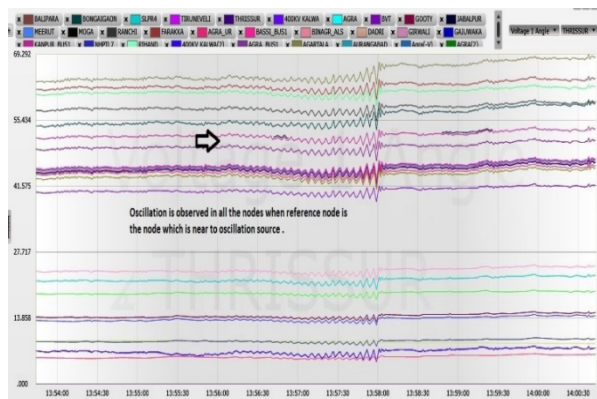


Figure 7: Wide area angular separation with the reference node near to the source of LFO. Oscillation can be observed in the entire system.

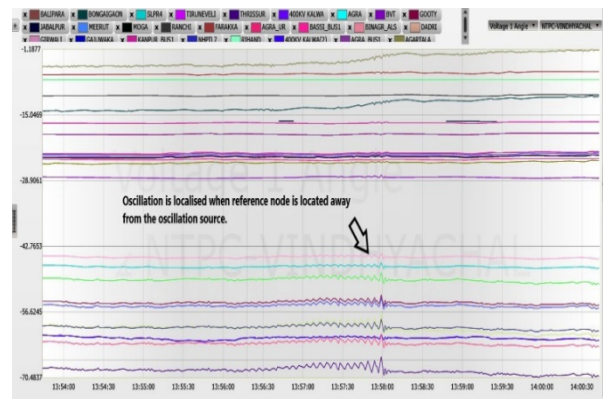


Figure 8: Wide area angular separation with the reference node away from the source of LFO. Source of oscillation and its localization can be observed.

2. Selection of wide area node pair for angular separation monitoring: One of the major advantages of WAMS system is the availability of angular separation between any two nodes in the system. It helps in identifying the system healthiness and stress at the various operating points. Baselining activities play a major role in determining the wide area node pairs [9]. In the Indian power system, node pairs were selected based on the following criteria:

1. Generation complex to Load complex
2. Power Corridors/Flow Gates
3. Power Corridors from One Region to Other.
4. Maximum Angular Separation in the Grid (wide distant node).

One example of the baselining activity is shown in Figure 9 and 10 for load generation wide area node pair. Similar exercises were done for various other angular node pairs used for monitoring.

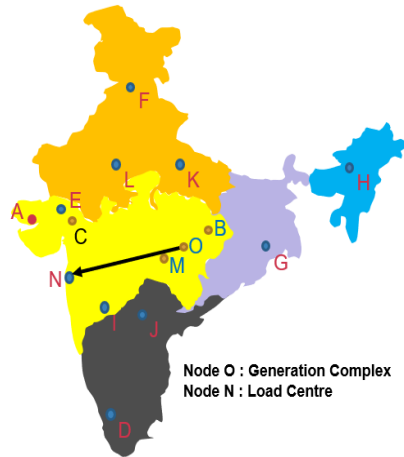


Figure 9: Wide area node pair between generation and load centre.

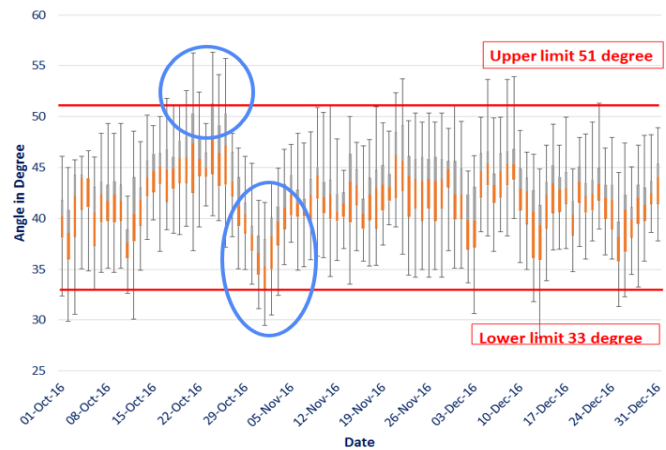


Figure 10: Wide area angular separation baselining for the generation and load node point shown in the adjacent figure.

3. Event detection setting and alarms segregation: Early warning situational awareness can be achieved through quick event detection on Synchrophasor data. It mainly helps in taking preventive action in immediately after events to avoid its cascading consequences. The event can be detected by detecting the sudden variation in monitored parameters like frequency, Positive Sequence Voltage Magnitude, Rate of Change Frequency (ROCOF) and Angle Difference. Based on observation from several events and their baselining, it is observed that the rate of change in frequency and positive sequence voltage, ROCOF and adjacent node Angle Difference signals can be configured for event detection through common settings for all PMUs at once globally. However, in the case of MW, MVAR signals individual event detection settings need to be configured. Sample setting for frequency, positive sequence voltage magnitude, rate of change and the angular difference are shown in Figure 11.

Magnitude Events / Default Magnitude Event Settings for Angle Difference	Magnitude Events / Default Magnitude Event Settings for Frequency	Magnitude Events / Default Magnitude Event Settings for d f / d t	Magnitude Events / ADAM_OIE 8-400BUS1_VPM
Upper Alarm (°) 30.0	Upper Alarm (Hz) 50.3	Upper Alarm (Hz/s) 0.5	Enabled <input checked="" type="checkbox"/>
Upper Alert (°) 28.0	Upper Alert (Hz) 50.2	Upper Alert (Hz/s) 0.3	Use Defaults <input checked="" type="checkbox"/>
Lower Alarm (°) -20.0	Lower Alarm (Hz) 49.8	Lower Alert (Hz/s) -0.3	Voltage Level 400 kV
Lower Alarm (°) -30.0	Lower Alert (Hz) 49.75	Lower Alarm (Hz/s) -0.5	Voltage Units pu
Alarm On (sec) 2.0	Alarm On (sec) 0.5	Alarm On (sec) 0.2	Upper Alarm (pu) 1.05
Alarm Off (sec) 120.0	Alarm Off (sec) 60.0	Alarm Off (sec) 2.0	Upper Alert (pu) 1.025
Alert On (sec) 2.0	Alert On (sec) 0.5	Alert On (sec) 0.5	Lower Alert (pu) 0.975
Alert Off (sec) 120.0	Alert Off (sec) 60.0	Alert Off (sec) 2.0	Lower Alarm (pu) 0.95
Save Cancel	Save Cancel	Save Cancel	Alarm On (sec) 0.0
			Alarm Off (sec) 120.0
			Alert On (sec) 0.0
			Alert Off (sec) 120.0
			Save Cancel

Figure 11: Typical default settings for detection of Magnitude events for Angle Difference, Frequency, ROCOF and Positive Sequence Voltage Magnitude.

4. Classification of Low frequency oscillation modes: The fine resolution time synchronized data with higher granularity helps in observing low frequency oscillation (LFO) in the power system in real time. However, in order to provide correct situational awareness of the oscillation, baselining activity of oscillation and tuning of the oscillation monitoring system has to be completed. This exercise was completed during the Synchrophasor pilot project where various LFO events were analyzed and documented to provide good insight. Few reports have been published on the LFO documenting the whole exercise which helped in the classification and damping criteria [3-4]. The above analysis has been utilized for tuning of the oscillation monitoring system (OMS) in URTDSM. The details of

URTDMS and its utilization after the baselining exercise has been explained in a separate paper by the author [10].

5. Visualization Display for operator situational awareness: There are various kinds of displays available for the system operator which includes the geographical display, single line diagram (SLD), trend & dial display and contour display. These displays help the operator in observing the power system with better visibility.

6. Training of System Operator: This is also one of the vital aspects in improving the utilization of URTDSM across the system operator at various levels of control centres. In order to improve the utilization of WAMS at various control centres across the country, a training module has been designed having various use cases for the Indian power system. This has helped in enhancing the utilization of URTDSM in the Indian power system.

SUMMARY

So, overall the paper has discussed the various aspect of design, implementation, PDC functionalities and its shortcomings and challenges faced in the URTDSM which is the large PMUs project ongoing in India. It has described the feasibility of dedicated High bandwidth communication through Optical network in existing infrastructure and its upgrade followed by usage of STAT and Time Quality as reported under C37.118 Protocol for understanding the phasor data correctness and associated Time synchronization issues. It also shows that unforeseen challenges like negative latency due to GPS Locked time drifted frame is difficult to handle after the implementation of the project. URTDSM project has also showcased that during event detection, some parameters are global while some are element-centric which needs baselining activities. In addition to all these issues, other issues in the area of utilization of this project for operational usages like the selection of reference node, selection of node pair for angle monitoring, oscillation monitoring engine setting, visualization and operator training has also been addressed in the paper. Overall, the project has facilitated a lot of challenges and the innovative solutions adopted by the design and operation team for its utilization.

Acknowledgment

The authors acknowledge the support and encouragement given by POSOCO management. The authors are indebted to POSOCO personnel for their inputs for the content in the paper. The views expressed in this paper are that of the authors and may not represent the views of the organization to which they belong.

BIBLIOGRAPHY

- [1]. POSOCO, "Synchrophasors Initiative in India", New Delhi, Tech.Rep. December 2013.
- [2]. POSOCO, "Synchrophasors Initiative in India", New Delhi, Tech.Rep. June 2012.
- [3]. POSOCO, "Report on Power System oscillations experienced in Indian Grid on 9th, 10th, 11th and 12th August 2014", New Delhi, Tech.Rep. Sept 2014.
- [4]. POSOCO, "Report on Low Frequency Oscillation in Indian Power System", New Delhi, Tech.Rep. March 2016.
- [5]. Report by PGCIL, "Unified Real Time Dynamic State Measurement (URTDMS)", February 2012, Online : http://www.cea.nic.in/reports/committee/scm/allindia/agenda_note/1st.pdf
- [6]. IEEE Std C37.118.1-2011, IEEE Standard for Synchrophasor Measurements for Power Systems.
- [7]. IEEE Guide for Phasor Data Concentrator Requirements for Power System Protection, Control, and Monitoring, " in IEEE Std C37.244-2013 , vol., no., pp.1-65, 10 May 2013.
- [8]. A. Derviskadić, P. Romano, M. Pignati and M. Paolone, "Architecture and Experimental Validation of a Low-Latency Phasor Data Concentrator," in IEEE Transactions on Smart Grid, vol. 9, no. 4, pp. 2885-2893, July 2018.
- [9]. Srinivas Chitturi, Sunil K. Patil, Chandan Kumar, Rajkumar Anumasula, Pradeep Kumar Sanodiya, Vivek Pandey, "Selection of Reference Node and Angular Baselining using Synchrophasors Measurement for Real Time Operation", NASPI WG Meet, March 2017, Online : https://www.naspi.org/sites/default/files/2017-03/02_Sanodiya_Selection_Reference_Node_Angular_Baselining_20170322.pdf
- [10]. C. Kumar *et al.*, "Detection of LFO and Evaluation of Damping Improvement Using Synchrophasor Measurement," 2018 IEEE PES Asia-Pacific Power and Energy Engineering Conference (APPEEC), Kota Kinabalu, 2018, pp. 701-706.